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L7: Entry 9 of 12

File: USPT

May 3, 1994

DOCUMENT-IDENTIFIER: US 5309258 A

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TITLE: Pattern image generation device for image processing system

Abstract Text (1):

A pattern image generation device which is able to generate various patterns by use of a RAM for processing ordinary image data and also is able to generate the patterns in a simple structure. The pattern image generation device includes an image conversion processor for converting an input image data signal to output a converted image data, the image conversion processor including rewritable memory and address controller for controlling a memory address of said memory, and an operation processor for controlling the operation of the image conversion processor.

Application Filing Date (1):19920911Brief Summary Text (10):

The IPS is a system which is used to input therein the read signals B, G and R from IIT 100, performs various kinds of data processings on the read signals in order to enhance the reproducibility of color, gradation, fineness and the like, selects the record signal of a develop process color from the record signals Y, M, C and K, converts the selected record signal into an on/off signal, and outputs the on/off signal to IOT 115. As shown in FIG. 8, the IPS includes an END conversion (Equivalent Neutral Density conversion) module 101 which adjusts (converts) the record signal into a grey balanced color signal; a color masking module 102 which matrix operates the read signals B, G and R to thereby convert the read signals into the record signals that correspond to the toner amounts of Y, M and C; a document size detection module 103 which detects a document size in pre-scanning and erases (erases the frame of) a platen color in document read scanning; a color conversion module 104 which converts a color specified in a given area in accordance with an area signal input from an area image control module; a UCR processing & black generation module 105 which generates K in a proper amount in order to prevent a color from being made impure and decreases Y, M and C equally in amounts according to the amount of K generated and also which performs a UCR processing on the K signals as well as the record signals Y, M and C in accordance with signals in a mono-color mode and a full color mode and gates the signals that are obtained after such UCR processing; a space filter 106 having a function to recover an unsharp color and a function to remove a moire; a TRC (Tone Reproduction Control) module 107 which performs a density adjustment, a contrast adjustment, a negative-positive reversal, color balance adjustment and other similar processings in order to improve reproducibility; a reduction and enlargement processing module 108 which performs a reduction and enlargement processing in a main scanning direction; a screen generator 109 which converts a gradation toner signal of a process color into a binary on/off toner signal and outputs the binary on/off toner signal; an IOT interface module 110, an area image control module 111 which includes an area generation circuit and a switch matrix; an edit control module which includes an area command memory 112, a color palette video switch circuit 113, a font buffer 114 and the like; and other similar modules.

Brief Summary Text (17):

A pattern image generation device for a color image processing system includes an image conversion processing means for converting an input image data signal to output a converted image data, the image conversion processing means including rewritable memory means and address control means for controlling a memory address of the memory means and an operation processing means for controlling the operation of the image conversion processing means, the address control means including a variable address generation means for generating a variable address signal in accordance with a synchronizing signal output from the operation processing means, and a signal select means for selecting one of said input image data signal, an address signal output from said operation processing means and the variable address signal in accordance with a control signal from the operation processing means, and wherein the operation processing means outputs to the memory means one of conversion data used to convert the input image data signal to be set in the memory means and predetermined pattern generation data to be set in the memory means in synchronization with the control signal, and the operation processing means controls the signal select means to select one of the input image data signal and the variable address signal.

Detailed Description Text (25):

The marker colors (three colors) detected from the image data by the color conversion & pallet 413 and a 4-bit signal in a closed area are sent to a density conversion/area generation circuit 405. The density conversion/area generation circuit 405 performs a binary processing, in which [1] is selected if there are present a given number of black pixels or more in 16 pixels, with a window of 4.times.4 by use of FIFOs 410a, 410b and 410c. That is, in the circuit 405, the density is converted from 400 spi into 100 spi. The thus generated marker signal (a closed loop or a marker dot) is written through a DRAM controller 402 into a plane memory 403 by the density conversion/area generation circuit 405.

Detailed Description Text (28):

The area command of 4 bits stored in the plane memory 403 is read out in synchronization with the output of the image data and is used to switch the parameters and the like of the filter 25, multiplier 26, TRC circuit 27, screen generation part 28 and the like through the image data processing system, ENL conversion circuit 15, matrix conversion circuit 16, selector 17, under density detection circuit 21 and area decoder 24 respectively shown in FIG. 3(a). When the area command is read out from the plane memory 403 and is used to perform the edit processing in the color conversion & pallet 413 and to switch the parameters in the image data processing system, the density conversion from 100 spi to 400 spi is necessary and such density processing is performed by the density conversion/area generation circuit 405. In the density conversion/area generation circuit 405, FIFOs 409a and 409b are used to provide a block of 3.times.3 and data interpolation is carried out in accordance with the block pattern, whereby the density is converted from 100 spi to 400 spi so as to prevent the corrugated boundaries of a closed loop curve, edit area and the like. Delay circuits 411a, 411b, IMFIFO 412 and the like are used to adjust a timing between the area command and image data.

CLAIMS:

1. A pattern image generation device for a color image processing system comprising:

an image conversion processing means for converting an input image data signal to output a converted image data, said image conversion processing means including rewritable memory means and address control means for controlling a memory address of said memory means; and

an operation processing means for controlling the operation of said image

conversion processing means;

said address control means including a variable address generation means for generating a variable address signal in accordance with a synchronizing signal output from said operation processing means, and a signal select means for selecting one of said input image data signal, an address signal output from said operation processing means and said variable address signal in accordance with a control signal from said operation processing means, and wherein said operation processing means outputs to said memory means one of conversion data used to convert said input image data signal to be set in said memory means and predetermined pattern generation data to be set in said memory means in synchronization with said control signal, and said operation processing means controls said signal select means to select one of said input image data signal and said variable address signal.

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